MANUAL OR OPTION SECTION

NAME: 560-5153 - E1/T1 FREQUENCY SYNTHESIZER MANUAL

APPROVALS

ENGINEER / ORIGINATOR	**D.T. McCALLUM/C. Bryan**
OTHER (A/R)	
DOCUMENT SERVICES	Perry M.

FILE NAME (include path)

I:\TCMANUAL\MANUALS\560\560-5XXX\5153.DOC

REVISION HISTORY

REVISION NUMBER	DATE
N/C	March 30, 1998
A	May 29, 1998
B	December 20, 1999
C	February 5, 2002
D	October 1, 2002

Model 560-5153
E1/T1 Frequency Synthesizer
(8, 64, 1544, and 2048 kHz)

SECTION ONE

1. FUNCTIONAL DESCRIPTION
1.1. PURPOSE OF EQUIPMENT
1.2. PHYSICAL SPECIFICATIONS
1.3. ENVIRONMENTAL SPECIFICATIONS
1.4. POWER REQUIREMENTS
1.5. FUNCTION SPECIFICATIONS
1.5.1. REF A, B, AND C INPUTS
1.5.2. LOOPBACK INPUT
1.5.3. OUTPUTS
1.5.4. CARD COMPATIBILITY

SECTION TWO

2. INSTALLATION AND OPERATION
2.1. HOT-SWAPPING
2.2. REMOVAL AND INSTALLATION
2.3. SETUP
2.3.1. REQUIRED SWITCH SETTINGS
2.3.2. OPTIONAL SWITCH SETTINGS
2.3.3. JUMPER SETTINGS
2.4. FAULT INDICATION
2.4.1. POWER SUPPLY / REFERENCE FAULT
2.4.2. CHANNELS A-F
2.4.3. INITIALIZATION FAULT
2.4.4. DETAILED FAULT AND CONFIGURATION STATUS VIA CPU

SECTION THREE

3. THEORY OF OPERATION
3.1. GENERAL INFORMATION
3.2. HARDWARE DESCRIPTION
3.3. DETAILED DESCRIPTION
3.3.1. PASSIVE COMBINER
3.3.2. POWER SUPPLY
3.3.3. VCOS
3.3.4. FPGA / CPU INTERFACE

SECTION FOUR

4. DETAILED DRAWINGS
4.1. 560-5153 DETAILED DRAWINGS / BILL OF MATERIALS

SECTION ONE

1. FUNCTIONAL DESCRIPTION

1.1. PURPOSE OF EQUIPMENT

The TrueTime 560-5153 E1/T1 Frequency Synthesizer is a plug-in option card for the Model 56000 DRC. This option card offers the user six independently configurable input/output channels that are configured by installing SILIOMs (Single-In-Line-Input/Output Modules) that can provide 1544 kHz and 2048 kHz outputs in AMI, CMOS SQUARE, RS-422 SQUARE, and SINE wave formats. They can also provide 8 kHz and 64 kHz outputs in CMOS SQUARE, and RS-422 SQUARE wave formats, as well as COMPOSITE CLOCK AMI and ALARM RELAY contacts. A single input module has been defined to accept a live T1 or E1 stream and extract the clock from it for use by AMI and other output modules. These modules resemble the 72 pin SIMMs used for PC memories and use the same type of connector.

The E1/T1 Frequency Synthesizer generates an output frequency that is locked to the external reference frequency distributed via REF A, B, or C on the backplane. The input frequency from the REF A, B, and C inputs (1, 5, or 10 MHz) is selectable by on-card DIP switches SW4-8. The reference is received via the passive combiner, which passes only the currently-highest priority reference to the synthesizer. If the currently highest priority reference is lost, the passive combiner shifts to the next-highest priority input and the synthesizer locks to the new reference. This is done without introducing any glitches on the output of the passive combiner.

In a system without a Fault Monitor CPU card, the E1/T1 Frequency Synthesizer card offers automatic REF A, B, C passive combiner operation as previously stated. When the E1/T1 card is used in a system that includes the Fault Monitor CPU card, the REF A, B, C inputs are also controlled by the CPU. When a REF A source's Fault Status is detected (monitored by the CPU), the REF A input on the E1/T1 card is disabled. The REF B and REF C inputs are operated similarly -- they are turned off whenever a Fault Status condition for that reference exists. The CPU's REF A, B, C control feature ensures that only a viable reference oscillator is used to drive the 560-5153 E1/T1 card.

The E1/T1 Frequency Synthesizer also has the capability of synchronizing AMI outputs to a live T1 or E1 stream in a loopback mode of operation. This mode requires that loopback operation be enabled on the AMI output cards affected and that a Clock Stripper input card be installed in one of the six I/O channels.

The input/output signals are delivered to external cables via the I/O card installed in the rear slot directly behind the E1/T1 synthesizer.

1.2. PHYSICAL SPECIFICATIONS

Dimensions:	0.8”w X 3.94”h X 8.66”d (2 cm X 10 cm X cm)
Weight:	Approximately ½ pound (¼ kg)

1.3. ENVIRONMENTAL SPECIFICATIONS

Operating Temp:	0° to +50°C
Storage Temp:	-40° to +85°C
Humidity:	Up to 95% relative, non-condensing
Cooling Mode:	Convection
Altitude:	Sea level to 10,000 ft.

1.4. POWER REQUIREMENTS

Voltage:	18-72 VDC
Power:	Depends on the number and type of SILIOMs installed, 1.7W with no SILIOMs installed.

1.5. FUNCTIONAL SPECIFICATIONS

1.5.1. REF A, B, AND C INPUTS

Signal Type:	Squarewave or Sinewave
Amplitude:	2-5 Vpp
Frequency:	1, 5, or 10 MHz (switch-selectable)

1.5.2. LOOPBACK INPUT

Signal Type:	AMI PER G.703 and G.704
Frequency:	E1 OR T1

1.5.3. OUTPUTS

Frequencies:	8, 64, 1544, 2048 kHz
Frequency Stability:	
Long-term:	Equal to reference on REF A, B, or C
Short-term:	< 1 $X10^{-9}$ (1 s avg, ref $1X10^{-10}$)
Signal Type(s):	Depends on SILIOM type(s) installed.

1.5.4. CARD COMPATIBILITY

Location:	Slot 1-17 with compatible I/O card in rear slot.
Compatibility:	See Card Compatibility Matrix.

SECTION TWO

2. INSTALLATION AND OPERATION

2.1. HOT SWAPPING

All cards, input cables, and output cables are hot swappable. It is not necessary to remove chassis power during insertion or removal. Hot swapping and reference-source changes are abrupt, the effects difficult to characterize; however, the system is designed to protect against permanent effects and minimize temporary effects of these events. Typically, adjacent-card hot swapping has a negligible effect on the E1/T1 Frequency Synthesizer. The effect of redundant power supply switch-over is also negligible.

The effect of a reference-source change is less predictable. The reference frequency is delivered via REF A, B, and C on the backplane. The E1/T1 Frequency Synthesizer receives the reference via the Passive Combiner. If the currently-highest priority reference is lost, the Synthesizer locks to the new reference. When the new reference is in phase with the old reference, the output frequency is affected by less than 1 part in 10^8 over a 1 second period. When the new reference is of opposite phase, the effect can approach 1 part in 10^6. The frequency-shift occurs relatively softly over a 100 ms period, minimizing any effect on downstream equipment. Note that hot swapping a local frequency source, such as an oscillator or fiber optic receiver, qualifies as a hot swap and reference-source change.

The effect of a reference-input perturbation that does not result in a reference-source change (e.g. - removing a cable that is not currently-highest priority) at the passive combiner also has an effect on the E1/T1 Frequency Synthesizer. This is due to the fact that the reference frequency used by the synthesizer is always a weighted sum of REF A, B, and C, and any change has some effect on the resultant waveform. The effect is usually negligible, but can approach 1 part in 10^8.

2.2. REMOVAL AND INSTALLATION

CAUTION: Individual components on this card are sensitive to static discharge. Use proper static discharge procedures during removal and installation.

Refer to CARD COMPATIBILITY section prior to installing new card.

To remove card, loosen the captive retaining hardware at the top and bottom of the assembly, then firmly pull on the handle at the bottom of the card. Slide the card free of the frame. Refer to the SETUP section for any required switch settings; or, set them identically to the card being replaced. Reinstall the card in the frame by fitting it into the card guides at

the top and bottom of the frame and sliding it in slowly, avoiding contact between bottom side of card and adjacent card front panel, until it mates with the connector. Seat card firmly to avoid contact bounce. Secure the retaining screws at the top and bottom of the card assembly.

2.3. SETUP

The setup of the 560-5153 E1/T1 Frequency Synthesizer card involves setting the following DIP switches:

2.3.1. REQUIRED SWITCH SETTINGS:

2.3.1.1. PASSIVE COMBINER SELECT SWITCHES (SW4-8)

These switches should all be set alike with no more than one switch position in each switch assembly set to the "ON" position. Additionally, Position 4 in each of these switch assemblies has no function. Position 1 "ON" equals 10 MHz, Position 2 "ON" equals 5 MHz, Position 3 "ON" equals 1 MHz.

2.3.2. OPTIONAL SWITCH SETTINGS:

2.3.2.1. OPTIONS SWITCH (SW1)

Except for Position 1, all of these switches should be set to the "OFF" position. Their use is reserved for future enhancements to the cards functionality. Position 1 selects the framing mode for the T1 data stream. When this switch is in the "ON" position it sets the framing mode to Extended Super Frame. When in the "OFF" position, the framing mode is D4/Super Frame.

2.3.2.2. OPTIONS SWITCH (SW2)

These switches should all be set to the "OFF" position. Their use is reserved for future enhancements to the cards functionality.

2.3.2.3. OPTIONS SWITCH (SW3)

These switches should all be set to the "OFF" position. Their use is reserved for future enhancements to the cards functionality.

2.3.3. JUMPER SETTINGS:

2.3.3.1. JTAG DAISY CHAIN JUMPERS (JP7-JP12)

These jumpers are used to close the JTAG chain when using the JTAG interface port for any empty SILIOM connector. The unit is shipped without jumper shunts installed since this option is not normally used in an operational system.

2.3.3.2. SILIOM OUTPUT CONFIGURATION JUMPERS (JP1-JP6)

Refer to the SILIOM manual for the card you are setting up for instructions on setting up JP1-JP6.

2.4. FAULT INDICATIONS

All indicators activate briefly following hot-insertion or power-up. This is a normal condition which occurs as the card configures itself. The following paragraphs describe operation during post power-up conditions.

2.4.1. POWER SUPPLY / REFERENCE FAULT

A continuously-flashing P/R LED indicates the loss of all reference inputs. A solid P/R LED indicates a local power supply failure. Loss-of-lock (blinking P/R LED) could be caused by either the input reference being grossly off-frequency or by a loss of all signals on REF A, B, and C (the second case being a special case of the first).

2.4.2. CHANNELS A-F

The Channel A through Channel F Fault indicators light when the associated output type SILIOM has detected a loss of its output or, in the case of an input type SILIOM, its input. Refer to the individual SILIOM manuals to determine what fault conditions can be detected.

2.4.3. INITIALIZATION FAULT

This is an on-card fault indicator which is not externally visible; although it can be seen by installing the card next to an empty slot. It indicates a failure of the card to initialize properly during power-up. Activation of this LED is accompanied by activation of all of the front panel indicators. Occasionally, this fault is caused by a temporary condition related to the cycling of power and can be cleared by a power or hot swap cycle. If this is unsuccessful, the card is defective.

2.4.4 DETAILED FAULT STATUS VIA CPU

The Fault Monitor CPU has access to detailed 560-5153 card status. This status is available via the Fault Monitor CPU serial port. When it is presented in a 2-byte format, with individual bit definitions as follows:

The Verbose report displays the Fault status. In this context, a reported fault indicates a problem. The Machine report, when used, reports the current status (settings) of the switches and faults in hexadeci
mal characters. Together, they pinpoint problems and help the technician view the switch settings on the cards without removing them.

2.4.5 VERBOSE REPORTS

The following is an example of a Fault Monitor CPU report in Verbose mode:

```
TrueTime 56000 Site 01
Automatic Reports Enabled
Periodic Reports Disabled
Primary Inputs Selected REFA No REFB No REFC Off PRI OK
SEC OK TER Off

1. Undefined        OK        Undefined      OK
2. Undefined        OK        Undefined      OK
3. 5153 XL2 LOCAL OSC FAULT 0007 Undefined OK
4. Undefined        OK        Undefined      OK
```

The above sample tells you that:
Automatic reports are enabled and Periodic reports are disabled. Primary inputs REF A and REF B are not bussing AUX REF. REF C is off. Primary and Secondary inputs OK, Tertiary is OFF.

Numbers 1-4 are slots (not all slots are shown in the example). Slots 1,2,and 4 are undefined (empty) and functional (OK).

Slot 3 is read as follows:
5153 is the abbreviation of the 560-5153 card. The fault reading is 0007.

2.4.6 MACHINE REPORTS

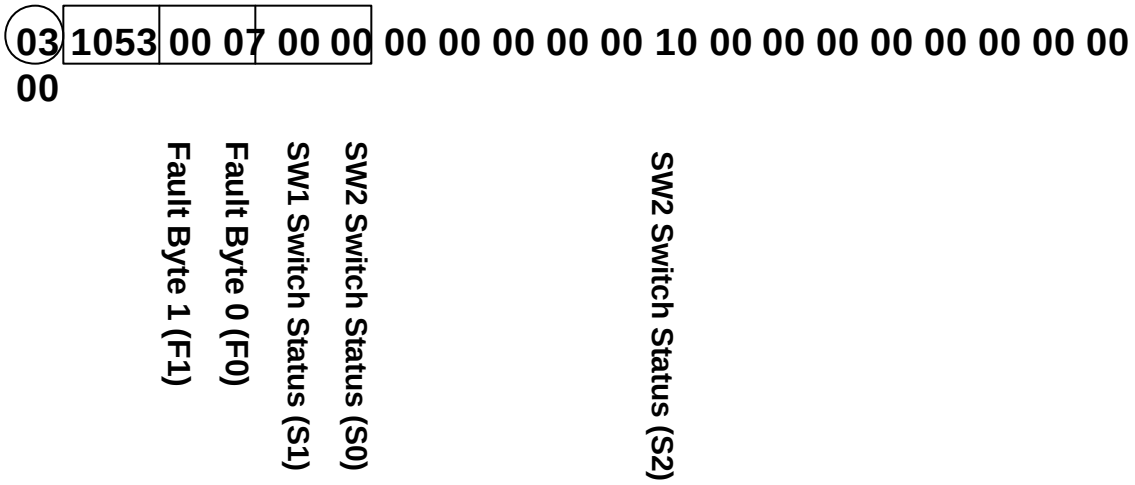
The Fault Monitor CPU has another serial output mode called machine report mode. This mode is usually used with a computer program to interrogate the 56000 system status.

The machine report mode displays hexadecimal (HEX) characters like the verbose mode report.

The following is an example of a Fault Monitor CPU report in Machine Mode:

TrueTime 56000 Site 01
AR1
PR10
P A1 B1 Co P1 S1 To
01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
02 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
03 10 53 00 07 0000 00 00 00 00 00 00 **10** 00 00 00 00 00 00 00 00 00
04 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
(card slots 05 through 14 HEX not shown)

Example from card slot 3 above:



Slot 3 shows that the Fault status is 0027 (F1, F0). The Status report read-out is 0000(S1, S0). The Status 2 read-out 10.

2.4.7 REPORT CONVERSIONS

This section deals with how to read and convert the Fault and Status read-outs using various tables and binary conversions. To decipher a Fault Status report, use Fig. A.
For Status reports (S1, S0) use Fig. B.

Fig. A

Spare	Spare	Spare	Alarm Ind.Signal*	Undefined	Undefined*	Undefined	Power Cycled	Undefined	Undefined	Output Fault F*	Output Fault E*	Output Fault D*	Output Fault C*	Output Fault B*	Output Fault A*
8	**4**	**2**	**1**	**8**	**4**	**2**	**1**	**8**	**4**	**2**	**1**	**8**	**4**	**2**	**1**
2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0
0	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*1*	*1*
Upper Byte High Nibble				Upper Byte Low Nibble				Lower Byte High Nibble				Lower Byte Low Nibble			
0				**0**				**0**				**7**			
Fault Status F1 Report								**Fault Status F0 Report**							

Key:

Above each 8,4,2,1 is the corresponding fault for that bit. For instance, above the 8 bit in the Upper byte/Low nibble reads Rub. Lockmon, which is the fault .

Shaded area
Informational only. The upper row: Bit value hex weights (8,4,2,1) The Lower row corresponds to the hex weight above. For instance, 2^3 is 8 in binary.
Each section of 8,4,2,1 is a nibble of either an Upper or Lower byte and separated for easy recognition. Each nibble = 4 bits and each byte = 8 bits. "04" is the F1 report, "07" the F0 report.

Non-shaded area
This area is used according with the report read-out after a report is converted to binary. The 0407 is an example from a report.

Always read the report from Upper (High) byte to Lower (Low) Byte.

***** Latched Fault Bit -- Reset Via Fault Monitor CPU.

Status (S1, S0, S2) Conversion Table **FIG. B**

STATUS REG 0	Bit	Bit Value	Switch	
Low	0	1	SW2-1	
Nibble	1	2	SW2-2	
Low	2	4	SW2-3	**0**
Byte	3	8	SW2-4	
High	4	1	SW3-1	
Nibble	5	2	SW3-2	
Low	6	4	SW3-3	**0**
Byte	7	8	SW3-4	
STATUS REG 1				
Low	0	1	Siliom Register X	
Nibble	1	2	Siliom Register X	
High	2	4	Siliom Register X	**0**
Byte	3	8	Siliom Register X	
High	4	1	Siliom Register X	
Nibble	5	2	Siliom Register X	
High	6	4	Siliom Register X	**0**
Byte	7	8	Siliom Register X	
STATUS REG 2				
Low	0	1	Always 0, Reserved	
Nibble	1	2	Always 0, Reserved	
Low	2	4	Always 0, Reserved	**0**
Byte	3	8	Always 0, Reserved	
High	4	1	ESF Selected SW1-1	
Nibble	5	2	Test SW1-2	
Low	6	4	Test SW1-3	**1**
Byte	7	8	Test SW1-4	

Notes: The settings listed under the Switch column are HIGH or ON. For instance, frequency has SW 1-1 and SW 1-2. If SW 1-1 is ON, SW 1-2 is presumed to be OFF (although there is no specific mention of this). For switches, a 1 = ON, 0 = OFF.

BINARY CONVERSION TABLE

Decimal	Displayed in report as	Binary
0	0	0
1	1	1
2	2	10
3	3	11
4	4	100
5	5	101
6	6	110
7	7	111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111

Binary:
1 = Fault/Switch On
0 = No Fault/Switch Off

Use the Binary Conversion table to convert a read-out from the monitor to binary. For instance, if the report read-out was 3C15, this would be:

11\1100\1\101 in binary.

USING THE FAULT STATUS REPORT (F0, F1)

The hex weight (fault importance) has been assigned 8, 4, 2, 1. Beneath each number is the corresponding fault. Use Fig. A. The report example read 000. The 0 is high byte/high nibble, the 4, high byte/low nibble, the 0, low byte/high nibble and 0, low byte/low nibble. Each nibble falls under a section on Fig. A, high to low or left to right.

Look at Fig. A. Below this is a sample read-out. This read-out would appear on the monitor when a Verbose report is requested. In the example, there are no faults in the upper byte/high nibble or in the lower byte/high nibble because both are zero (0). In the upper byte/low nibble, a 0 is reported. However, In the lower byte/low nibble a 0 is reported.

Thus, in Status report 1 (S1) , there are no errors reported.

USING THE STATUS REPORT (S2)

The method used for reading the Fault report is the same when reading the Status report. Refer to Fig. B.

The report readout for the Status 2 report is 10.

Using the read-out, 10, but because the table is different, the 1 is located at the high nibble\low byte of Status Reg 2. The 0 is in the low nibble\low byte section of S2

1 = Active, 0 = Not active.

Since we have a 1 , reading from low byte\low nibble(from top to bottom) in Status 2, the current items are active:

ESF Selected SW1-1	1
Test SW1-2	0
Test SW1-3	0
Test SW1-4	0

Each of the four nibbles is grouped by category for easy visual identification of an offending fault. Each nibble has 15 possible fault combinations. All faults are asserted as a logic 1. The faults are latched on the Oscillator card and must be cleared by the 560-5179-1 Fault Monitor CPU “CL” command

QUICK REFERENCE SHEET FOR READING FAULT AND STATUS REPORTS

1. Run a report. This is a portion of a sample Machine report.

TrueTime 56000 Site 01
AR1
PR10
P A1 B1 Co P1 S1 To
01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
02 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
03 10 53 00 07 0000 00 00 00 00 00 00 **10** 00 00 00 00 00 00 00 00 00
04 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
(card slots 05 through 14 HEX not shown)

0007 is the Fault Status read-out
0000 is the Status read-out report
10 is Status 2 register read-out

00 = Fault Status 1 (F1) report
00 = Fault Status 0 (F0) report
00 = Status 1 (S1) report
00 = Status 0 (S0) report
10 = Status 2 (S2) report

03 1053 00 07 00 00 00 00 00 00 00 10 00 00 00 00 00 00 00 00 00

Fault Byte 1 (F1)
Fault Byte 0 (F0)
SW1 Switch Status (S1)
SW2 Switch Status (S0)
SW2 Switch Status (S2)

What's in a number?

0 4 0 7

High Byte High Nibble
High Byte Low Nibble
Low Byte High Nibble
Low Byte Low Nibble

2. When required, convert Decimal to Binary using the Binary Conversion Table.

BINARY CONVERSION TABLE

Decimal	Displayed in report as	Binary
0	0	0
1	1	1
2	2	10
3	3	11
4	4	100
5	5	101
6	6	110
7	7	111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111

Binary:
1 = Fault/On/Active
0 = No Fault/Off/Not Active

SECTION THREE

3. THEORY OF OPERATION

3.1. GENERAL INFORMATION

This section contains a detailed description of the circuits used on the E1/T1 Frequency Synthesizer card. Use these descriptions in conjunction with the drawings in SECTION FOUR.

3.2. HARDWARE DESCRIPTION

The E1/T1 Frequency Synthesizer incorporates a Passive Combiner, a DC-to-DC Converter, three phase-locked VCOs, and up to six SILIOMs

3.3. DETAILED DESCRIPTION

Reference drawing 560-5153.

3.3.1. PASSIVE COMBINER (Sheet 8)

The passive combiner is a circuit that strives to always output the desired signal, derived from the three separate inputs REF A, B, and C. The passive combiner minimizes any switching transient or glitch when one or two of the inputs are lost. It is composed of three input filter sections, three high speed comparators, a weighting network and a passive combining network. The filters and the combining network employ tuned circuits and therefore have to have their values adjusted depending on the required input frequency of either 1, 5, or 10 MHz. This is accomplished by the use of SW6 through SW8, which are 4PST DIP switches. The input filters and the comparators serve to produce a very clean square wave with very good symmetry. These square waves are then buffered and applied to the weighting network where they are summed with different weights in order to give the primary source the greatest influence on the final result. This summing results from an interaction between the weighting network and the combining network which is composed of a parallel resonant tank and a series resonant tank. These tanks are tuned slightly off center, lowering the Q, so that amplitude variations are minimized when input signals are changed. The final output voltage is then buffered and squared to produce the final signal called FREQIN.

3.3.2. POWER SUPPLY (Sheet 4)

The DC-to-DC Converter, PS1, converts 48 VDC backplane power to local ±5 VDC power. The outputs are fully-isolated from the backplane power and referenced to signal GND on the E1/T1 Synthesizer card. Backplane power is supplied via a Polyswitch

fuse device F1, diode D1 and a Pi-section L-C filter comprised of C80, C82, and L17. The poly-fuse protects the backplane power bus from internal DC-to-DC shorts. The diode protects the card from a voltage polarity reversal in the event of an installation error while wiring the chassis to an external DC power source. During normal operation, the L-C filter minimizes switching noise coupled back into the backplane power bus. During live-extraction, the 0.1 uF capacitor absorbs the inductive-kick of the opened circuit, minimizing contact-arcing. The -5 VDC output of the supply is loaded with R83 and R84, providing a minimum load to improve output voltage regulation.

3.3.3. VCOS (Sheet 5, 7, & SIGPLAN)

The card is equipped with three VCOs, operating at 10, 8.192, and 12.352 MHz. The 10 MHz VCO is phase locked to a 1 MHz reference frequency that is derived from REF A, B, and C inputs (FREQIN). The FPGA provides a divider and phase-comparator for the FREQIN signal and the 10 MHz on-board oscillator, as well as a frequency detection circuit. The frequency detection circuit monitors the FREQIN signal and determines whether it is 1, 5, or 10 MHz. It then selects the proper divide ratio to divide FREQIN by in order to provide 1 MHz to MIXER 6. The filtered phase comparison output from the loop filter integrator (FILTER 6) connects to the voltage control input on the 10 MHz VCTCXO (X1) closing the loop. The 10 MHz output is the clock source or reference for the rest of the synthesizer. Note that if all external frequency sources are lost, that this oscillator will continue to run and will serve as the on board reference. It is temperature compensated and provides a stability of about 2.5 PPM.

The FPGA also provides dividers and two phase comparators (MIXER 4 and MIXER 5) for the 8.192 MHz signal. After dividing the 8.192 MHz frequency by four to develop the 2.048 MHz E1 clock, the FPGA divides that frequency by two to generate a 1024 kHZ signal which is applied to MIXER 4. The other Input to MIXER 4 is 1000 kHZ obtained from dividing the 10 MHz VCO output by ten. MIXER 4s' output is fed out of the FPGA to a low pass filter, FILTER 4, which passes the 24 kHZ difference frequency of MIXER 4 back to the FPGA. There it is divided by six to yield 4 kHZ which is applied to MIXER 5. The other input of MIXER 5 is derived by dividing the VCO 10 MHz by 2500. MIXER 5s' output is fed out of the FPGA to a low pass filter and integrator (U6), FILTER 5, which passes the 0 HZ (at lock) difference frequency of MIXER 5 to the voltage control input on the 8.192 MHz VCXO (X3,U16) closing the loop. Thus the E1 signal is locked to the 10 MHz VCTCXO
The FPGA also provides dividers and three phase comparators (MIXER 1, 2, and 3) for the 12.352 MHz signal. The FPGA divides the 12.352 MHz frequency by eight to develop the 1.544 MHz T1 clock. The FPGA multiplies the 12.352 MHz signal by two to

generate a 24.704 MHz signal which is then divided down to yield the composite clock components CCLO and CCHI as well as 64 kHZ and 8 kHZ outputs. 12.352 MHz is also applied to MIXER 1. The other input to MIXER 1 is 10 MHz obtained from the 10 MHz VCO. MIXER 1s' output is fed out of the FPGA to a low pass filter, FILTER 1, which passes the 2352 kHZ difference frequency of MIXER 1 back to the FPGA where it is applied to MIXER 2. The other input of MIXER 2 is derived by dividing the VCO 10 MHz by 4 to yield 2500 kHZ. MIXER 2s' output is fed out of the FPGA to a low pass filter, FILTER 2, which passes the 148 kHz difference frequency of MIXER 2 back to the FPGA where it is divided by 74 and then applied to MIXER 3. The other input of MIXER 3 is derived by dividing the VCO 10 MHz by 5000 to yield 2 kHz. MIXER 3s' output is fed out of the FPGA to a low pass filter, FILTER 3, and integrator (U7:B), which passes the 0 Hz (at lock) difference frequency of MIXER 3 to the voltage control input on the 12.352 MHz VCXO (X2,U17) closing the loop. Thus the T1 signal is locked to the 10 MHz VCTCXO.

3.3.4. FPGA / CPU INTERFACE (Sheets 4, 5, & 6)

FPGA U4 provides the timing and control signals for the E1/T1 synthesizer. U14 holds the configuration data for the FPGA. DS8 will go on and stay on if the FPGA fails configuration for any reason. The timing and control signals are routed to a 1X6 array of connectors on the card into which are installed the required SILIOMs. In a system that includes a Fault Monitor/CPU assembly, the FPGA is also the interface between the E1/T1 Frequency Synthesizer and the CPU. Certain features can only be utilized via the CPU.

SECTION FOUR

4. DETAILED DRAWINGS

While detailed drawings concerning the design of the card are provided herein, it is strongly urged that no attempt be made to repair the card in the field. This is due to the fact that the card is constructed mainly of surface mounted components that are very difficult to repair successfully without the use of special equipment and training.

4.1. 560-5153 DETAILED DRAWINGS / BILL OF MATERIALS